

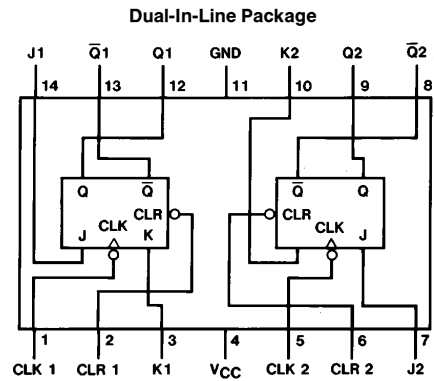
DM54LS73A/DM74LS73A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J

and K inputs is allowed to change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the levels of the other inputs.

Connection Diagram



TL/F/6372-1

Order Number DM54LS73AJ, DM54LS73AW, DM74LS73AM or DM74LS73AN
See NS Package Number J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	↓	L	L	Q_0	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	\bar{Q}_0

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↓ = Negative going edge of pulse.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM54LS73A			DM74LS73A			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			−0.4			−0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
f _{CLK}	Clock Frequency (Note 2)	0		30	0		30	MHz
f _{CLK}	Clock Frequency (Note 3)	0		25	0		25	MHz
t _w	Pulse Width (Note 2)	Clock High	20		20			ns
		Preset Low	25		25			
		Clear Low	25		25			
t _w	Pulse Width (Note 3)	Clock High	25		25			ns
		Preset Low	30		30			
		Clear Low	30		30			
t _{SU}	Setup Time (Notes 1 and 2)	20 ↓			20 ↓			ns
t _{SU}	Setup Time (Notes 1 and 3)	25 ↓			25 ↓			ns
t _H	Hold Time (Notes 1 and 2)	0 ↓			0 ↓			ns
t _H	Hold Time (Notes 1 and 3)	5 ↓			5 ↓			ns
T _A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	DM54	2.5	3.4	V
			DM74	2.7	3.4	
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	DM54		0.25	V
			DM74		0.35	
			$I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$	DM74		
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ $V_I = 7\text{V}$	J, K		0.1	mA
			Clear		0.3	
			Clock		0.4	
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7\text{V}$	J, K		20	μA
			Clear		60	
			Clock		80	
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4\text{V}$	J, K		-0.4	mA
			Clear		-0.8	
			Clock		-0.8	
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	DM54	-20	-100	mA
			DM74	-20	-100	
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 3)		4	6	mA

Switching Characteristics

at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$ (See Section 1 for Test Waveforms and Output Load)

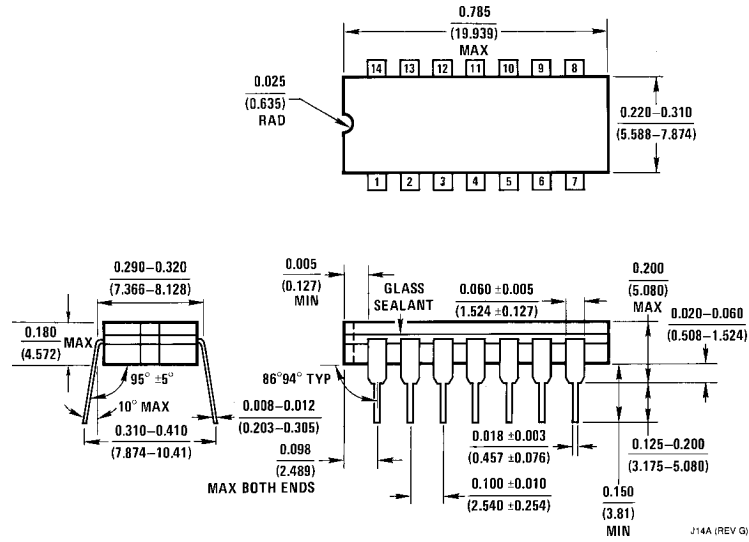
Symbol	Parameter	From (Input) To (Output)	$R_L = 2 \text{ k}\Omega$				Units
			$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to \bar{Q}		20		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or \bar{Q}		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or \bar{Q}		20		28	ns

Note 1: All typicals are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state, an equivalent test may be performed where $V_O = 2.25\text{V}$ and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock is grounded.

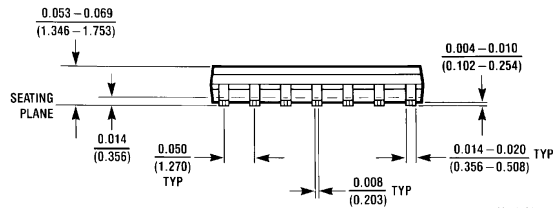
Physical Dimensions inches (millimeters)



14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS73AJ
NS Package Number J14A

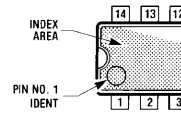
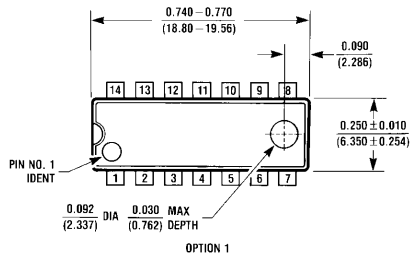
J14A (REV G)

Physical Dimensions inches (millimeters) (Continued)

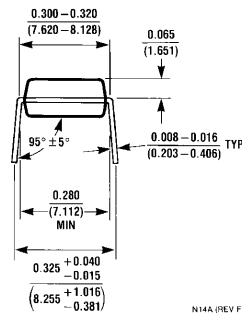
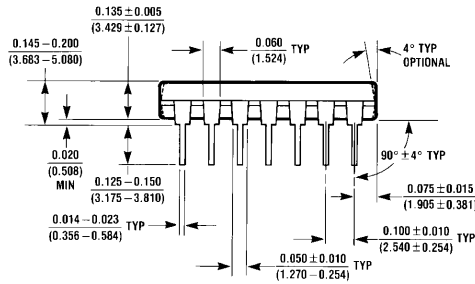


M14A (REV HI)

14-Lead Small Outline Molded Package (M)
Order Number DM74LS73AM
NS Package Number M14A



OPTION 02



N14A (REV F)

14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS73AN
NS Package Number N14A

**DM54LS73A/DM74LS73A Dual Negative-Edge-Triggered
Master-Slave J-K Flip-Flops with Clear and Complementary Outputs**

Physical Dimensions inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)
Order Number DM54LS73AW
NS Package Number W14B**

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