National Semiconductor

January 1988

MM54HC4543/MM74HC4543 BCD-to-7 Segment Latch/Decoder/Driver for Liquid Crystal Displays

General Description

The MM54HC4543/MM74HC4543 BCD-to-7 segment latch/decoder/driver utilize advanced silicon-gate CMOS technology, and can be used either as a high speed decoder or as a display driver. This circuit contains a 4-bit latch, BCD-to-7 segment decoder, and 7 output drivers. Data on the input pins flow through to the output when the LATCH ENABLE (LE) is high and is latched on the high to low transition of the LE input. The PHASE input (PH) controls the polarity of the 7 segment outputs. When PH is low the outputs are true 7 segment, and when PH is high the outputs are inverted 7 segment. When the PHASE input is driven by a liquid crystal display (LCD) backplane waveform the segment pins output the correct segment waveform for proper LCD AC drive voltages.

In addition a BLANKING INPUT (BI) is provided, which will blank the display.

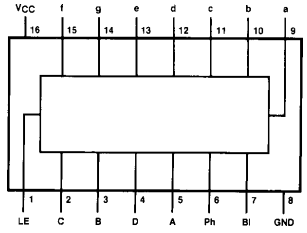
The MM54HC4543/MM74HC4543 are functionally and pinout equivalent to the CD4543BC/CD4543BM and the MC14543BA/MC14543BC. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 60 ns
- Supply voltage range: 2–6V
- Maximum input current: 1 μA
- Maximum quiescent supply current: 80 μA (74HC)
- Display blanking
- Low dynamic power consumption

Connection Diagram

Dual-In-Line Package



TL/F/5128–1

Top View

Order Number MM54HC4543 or MM74HC4543

Display Format

TL/F/5128–2

Truth Table

Inputs							Outputs							
LE	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	**							**
†	†	H	†				Inverse of Output Combinations Above							Display as above

X — don't care

† = same as above combinations

* = for liquid crystal readouts, apply a square wave to Ph.

** = depends upon the BCD code previously applied when LE—H

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 0.4$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 0.52$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 0.4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 0.52$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

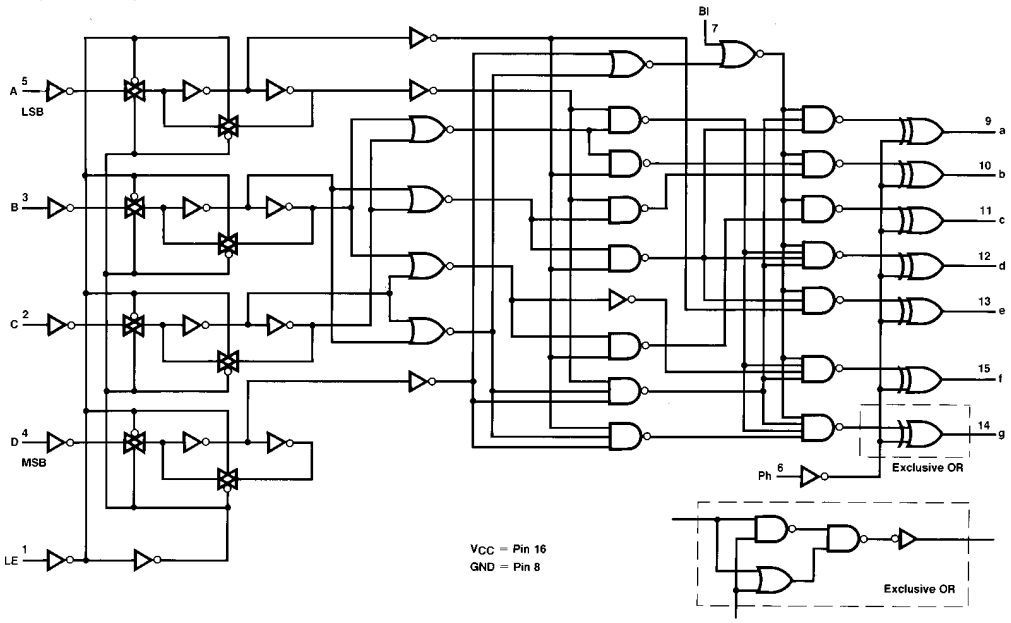
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data LE, BI, Ph to Output		60	100	ns
t_s	Minimum Setup Time LE to Data			20	ns
t_H	Minimum Hold Time Data to LE			10	ns
t_W	Minimum LE Pulse Width			16	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data LE, Ph, BI to Output		2.0V	300	600	760	895	ns
			4.5V	60	120	151	179	ns
			6.0V	51	102	129	152	ns
t_s	Minimum Setup Time LE to Data		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Data to LE		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		9	11	13	ns
t_W	Minimum LE Pulse Width		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

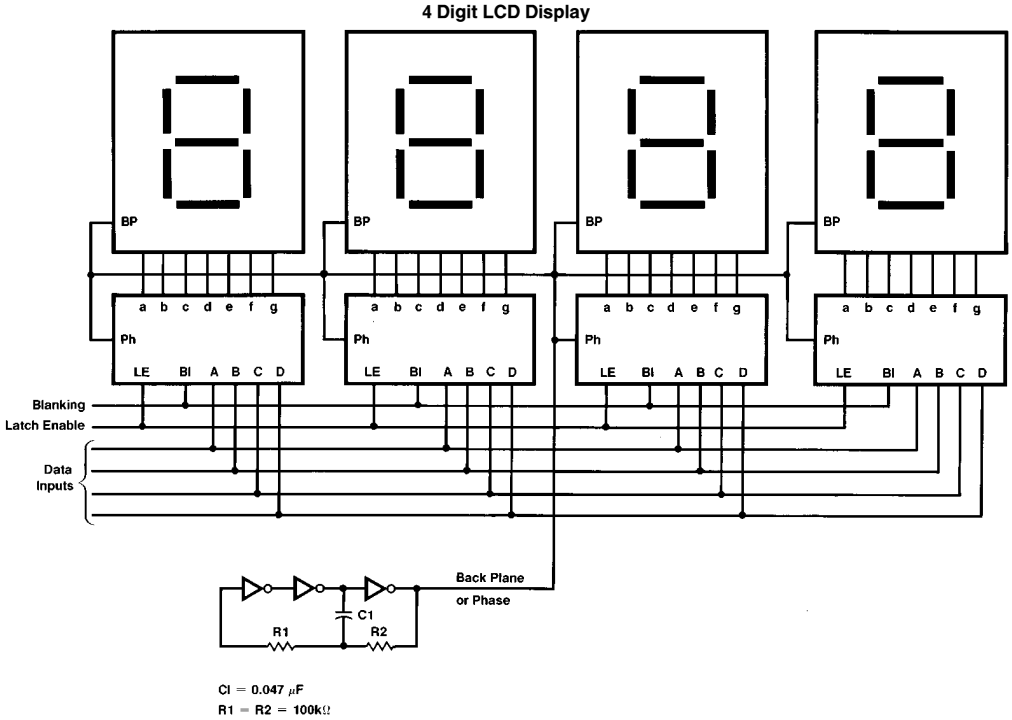
Logic Diagram



TL/F/5128–3

Typical Applications

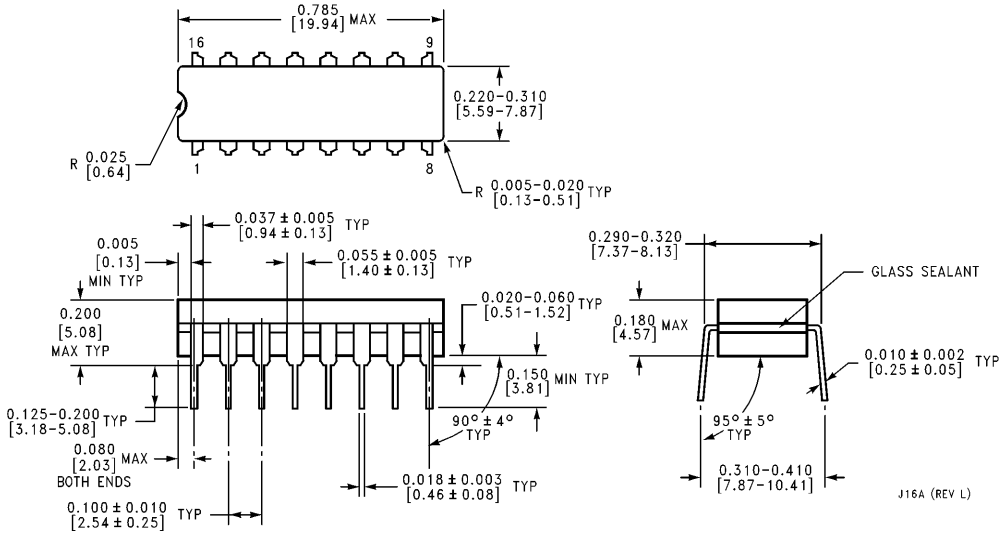
4 Digit LCD Display



C1 = 0.047 μF
R1 = R2 = 100kΩ

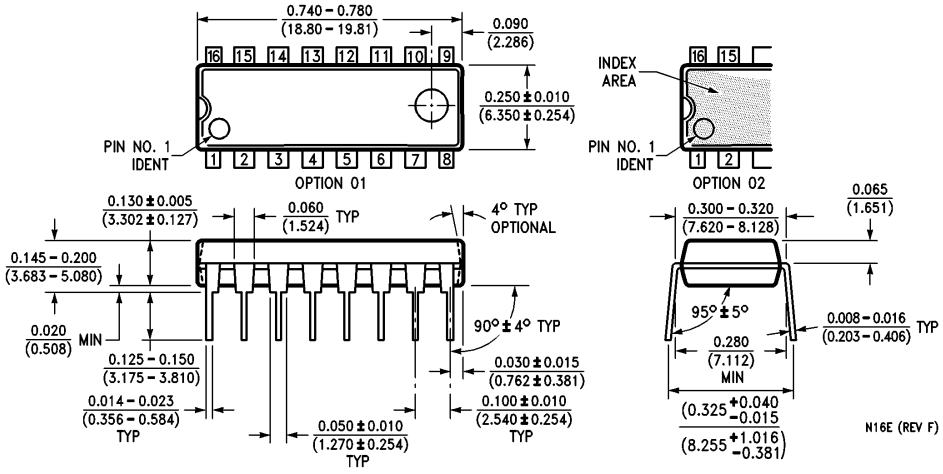
TL/F/5128–4

Physical Dimensions inches (millimeters)



Dual-In-Line Package
Order Number MM54HC4543J or MM74HC4543J
NS Package J16A

Physical Dimensions inches (millimeters) (Continued)



Order Number MM74HC4543N
NS Package N16E

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