National Semiconductor

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MM54HC620/MM74HC620 Inverting Octal TRI-STATE® Transceiver MM54HC623/MM74HC623 True Octal TRI-STATE Transceiver

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General Description

These TRI-STATE bi-directional buffers utilize advanced silicon-gate CMOS technology and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption and high noise immunity usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending on the logic levels at the enable inputs. Both buses can be isolated from each other with proper logic levels at the enable inputs. When GAB is taken high and GBA is taken low, these devices store the states presently appearing at the data inputs. The 8-bit codes appearing on the two sets of buses will be indentical for the 623 option or complimentary for the 620 option.

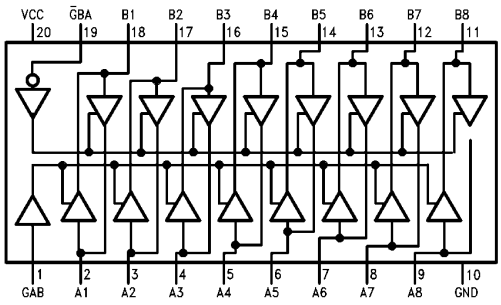
These devices can drive up to 15 LS-TTL loads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delays: 13 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 80 μA maximum (74HC series)
- TRI-STATE outputs for connection to system buses
- High output drive: 6 mA (minimum)

Connection Diagrams

Dual-In-Line Package

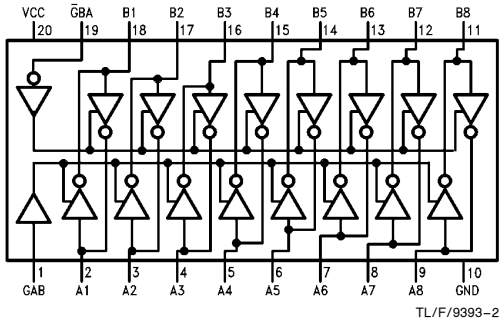


TL/F/9393–1

Top View

Order Number MM54HC623 or MM74HC623

Dual-In-Line Package



TL/F/9393–2

Top View

Order Number MM54HC620 or MM74HC620

Truth Table

Enable Inputs		Operation	
$\overline{G}$BA	GAB		
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	L	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

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 TL/F/9393

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage DIR and $\overline{G}$ pins (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{IN}, V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40°C to +85°C	54HC T_A = −55°C to +125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Input Leakage Current ($\overline{G}$ and DIR)	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND Enable $\overline{G}$ = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $t_r = t_f = 6$ ns

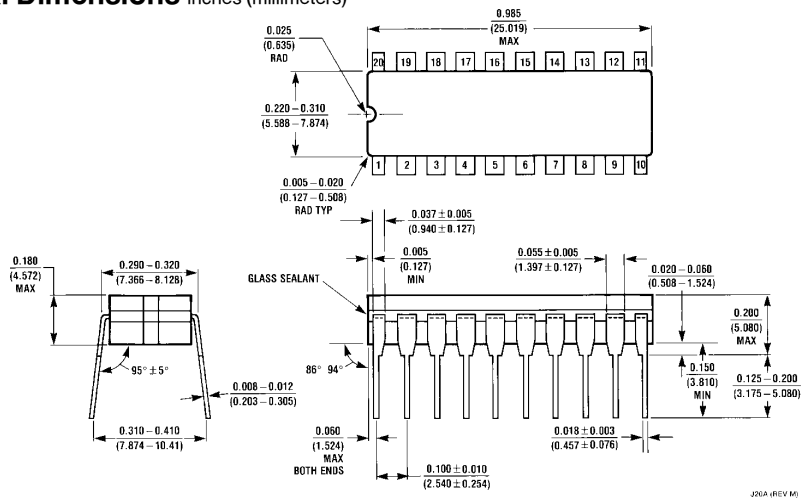
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 45$ pF		15	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1\ k\Omega$ $C_L = 45$ pF		31	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1\ k\Omega$ $C_L = 5$ pF		18	ns

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified

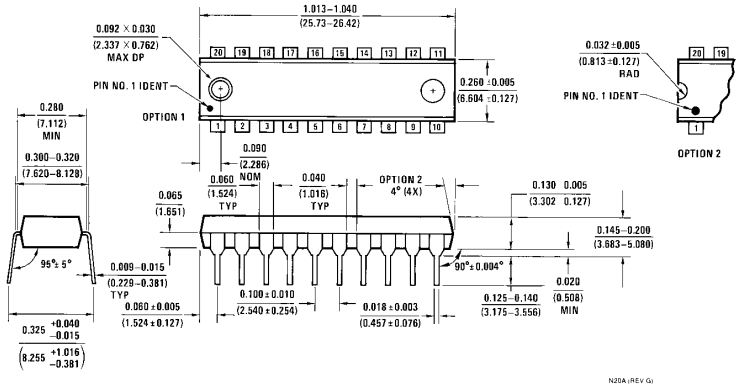
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40°C$ to $+85°C$	54HC $T_A = -55°C$ to $+125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 50$ pF	2.0V		85	105	130	ns
		$C_L = 150$ pF	2.0V		105	130	160	ns
		$C_L = 50$ pF	4.5V		17	21	26	ns
		$C_L = 150$ pF	4.5V		21	26	32	ns
		$C_L = 50$ pF	6.0V		14	18	22	ns
		$C_L = 150$ pF	6.0V		18	22	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L = 1\ k\Omega$						
		$C_L = 50$ pF	2.0V		170	215	255	ns
		$C_L = 150$ pF	2.0V		195	245	295	ns
		$C_L = 50$ pF	4.5V		34	43	51	ns
		$C_L = 150$ pF	4.5V		39	49	59	ns
		$C_L = 50$ pF	6.0V		29	37	43	ns
		$C_L = 150$ pF	6.0V		33	42	50	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1\ k\Omega$ $C_L = 50$ pF	2.0V		130	165	195	ns
			4.5V		26	33	39	ns
			6.0V		22	28	33	ns
t_{THL}, t_{TLH}	Output Rise and Fall Time	$C_L = 50$ pF	2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	$\overline{G}BA$, $GAB = V_{IL}$		120				pF
		$\overline{G}BA = V_{IH}$, $GAB = V_{IL}$		12				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
$C_{IN/OUT}$	Maximum Input/Output Capacitance, A or B			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54HC620, MM54HC623, MM74HC620 or MM74HC623
NS Package Number J20A



Molded Dual-In-Line Package (N)
Order Number MM54HC620, MM54HC623, MM74HC620 or MM74HC623
NS Package Number N20A

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