

5475/DM5475/DM7475 Quad Latches

General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q input when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high. These latches feature complementary Q and \overline{Q} outputs from a 4-bit latch and are available in 16-pin packages.

Features

Connection Diagram Function Table (Each Latch) **Dual-In-Line Package** Inputs Outputs ENABLE D Q Q G ō2 GND កិន 01 02 03 Q4 н н L L 12 15 14 13 11 10 9 16 н н н L Х L Q₀ \overline{Q}_0 H = High Level, L = Low Level, X = Don't Care, Q0 = The Level of Q Before the Highto-Low Transition of G 3 6 8 2 4 5 7 ENABLE 3-4 ______ Ō1 D1 D2 Vcc D3 D4 TI /F/6527-1 Order Number 5475DMQB, 5475FMQB, DM5475J, DM5475W or DM7475N See NS Package Number J16A, N16E or W16A Logic Diagram (Each Latch) 75 то ς 00 OTHER LATCH ENABLE DATA TL/F/6527-2

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Alternate Military/Aerospace device (5475) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	-55°C to +125°C
DM74	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	-65° C to $+150^{\circ}$ C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		DM5475			DM7475		Units
Cymbol	i alameter	Min	Nom	Max	Min	Nom	Max	onito
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
VIH	High Level Input Voltage	2			2			V
VIL	Low Level Input Voltage			0.8			0.8	V
IOH	High Level Output Current			-0.4			-0.4	mA
I _{OL}	Low Level Output Current			16			16	mA
t _W	Enable Pulse Width (Note 4)	20			20			ns
ts∪	Setup Time (Note 4)	20			20			ns
t _H	Hold Time (Note 4)	5			5			ns
Τ _Α	Free Air Operating Temperature	-55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conc	litions	Min	Typ (Note 1)	Мах	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I =$	= -12 mA			-1.5	V
V _{OH}	High Level Output Voltage	$V_{CC} = Min, I_{OH}$ $V_{IL} = Max, V_{IH}$	•	2.4	3.4		V
V _{OL}	Low Level Output Voltage	$\begin{array}{l} V_{CC} = Min, I_{OL} \\ V_{IH} = Min, V_{IL} \end{array}$			0.2	0.4	V
Ιį	Input Current @ Max Input Voltage	$V_{CC} = Max, V_{I}$	= 5.5V			1	mA
IIH	High Level Input Current	$V_{CC} = Max, V_I$	= 2.4V			80	μΑ
IIL	Low Level Input Current	$V_{CC} = Max, V_I$	= 0.4V			-3.2	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	DM54	-20		-55	mA
			DM74	-18		-55	
Icc	Supply Current V _{CC} = Max	V _{CC} = Max	DM54		32	46	mA
		(Note 3)	DM74		32	50	

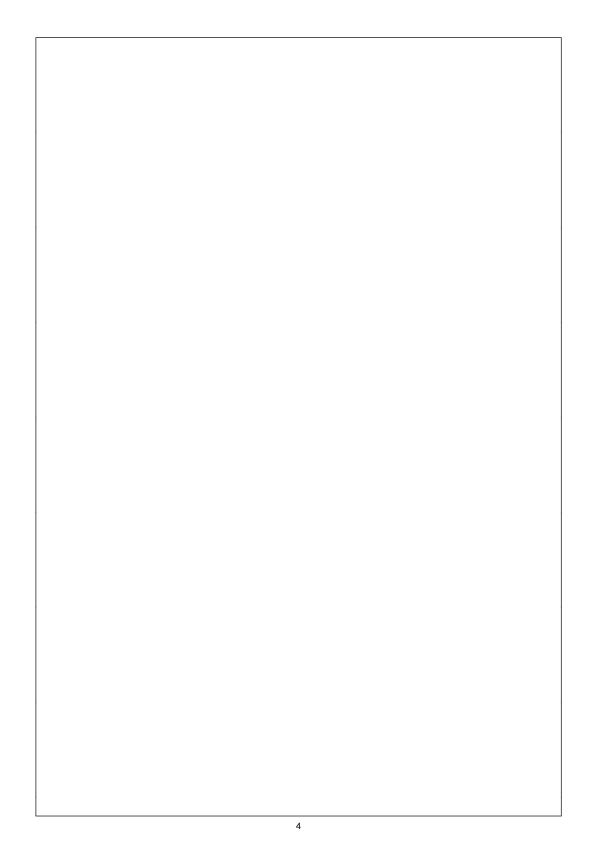
Note 1: All typicals are at V_{CC}\,=\, 5V, T_A = 25°C.

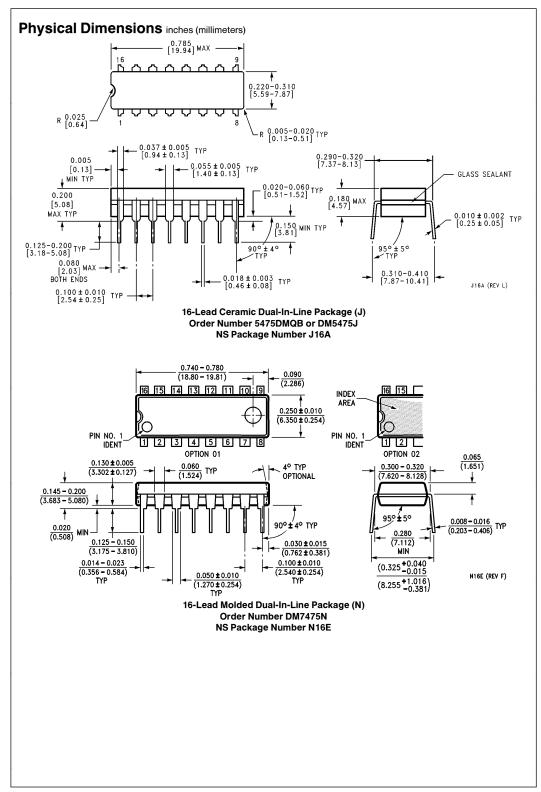
Note 2: Not more than one output should be shorted at a time.

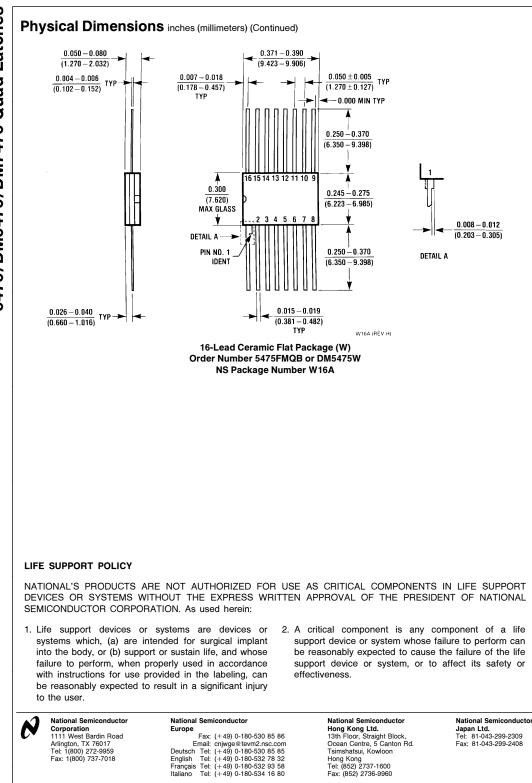
Note 3: $I_{\mbox{CC}}$ is measured with all inputs grounded and all outputs open.

Note 4: $T_A = 25^{\circ}C$ and $V_{CC} = 5V$.

Symbol	Parameter	From (Input) To (Output)	$R_{L} = 400\Omega$ $C_{L} = 15 \text{ pF}$		Units
			Min	Мах	
t _{PHL}	Propagation Delay Time High to Low Level Output	D to Q		25	ns
t _{PLH}	Propagation Delay Time Low to High Level Output	D to Q		30	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	D to \overline{Q}		15	ns
t _{PLH}	Propagation Delay Time Low to High Level Output	D to \overline{Q}		40	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	G to Q		15	ns
t _{PLH}	Propagation Delay Time Low to High Level Output	G to Q		30	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	G to \overline{Q}		15	ns
t _{PLH}	Propagation Delay Time Low to High Level Output	G to \overline{Q}		30	ns







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